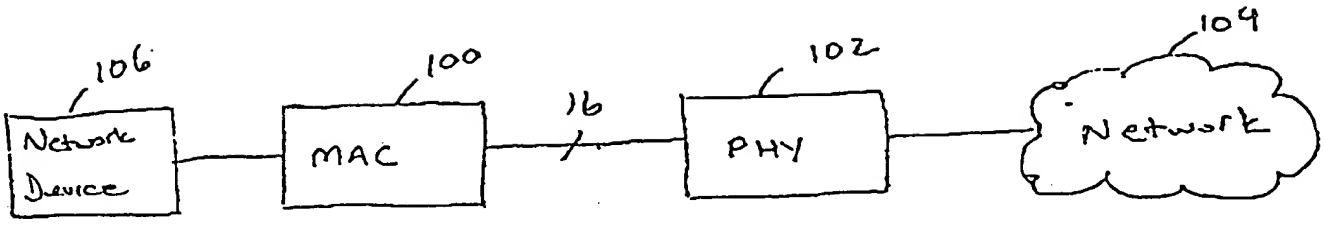

Figure 1A

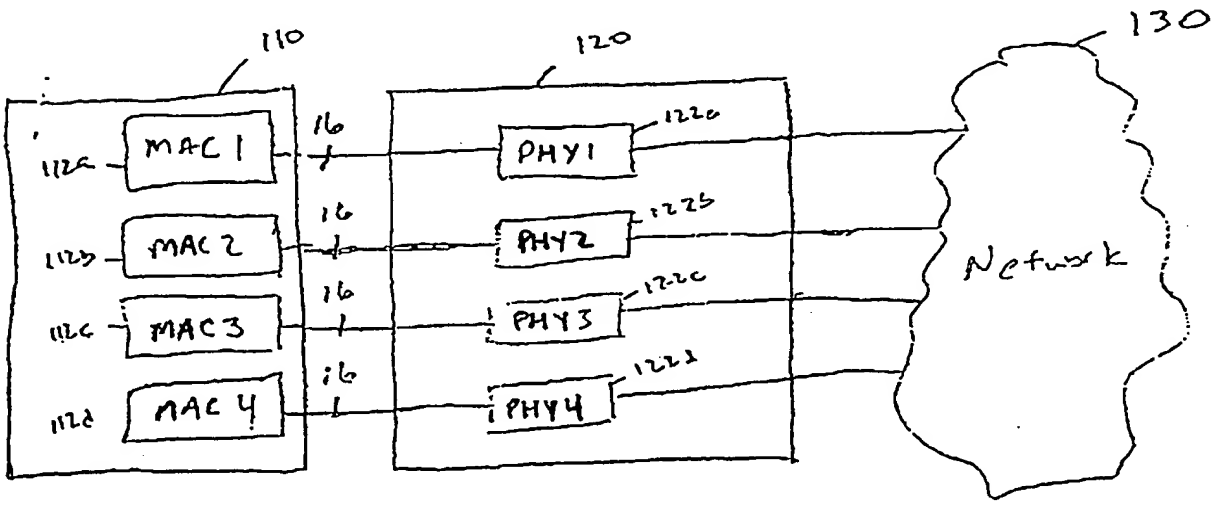

Figure 1B

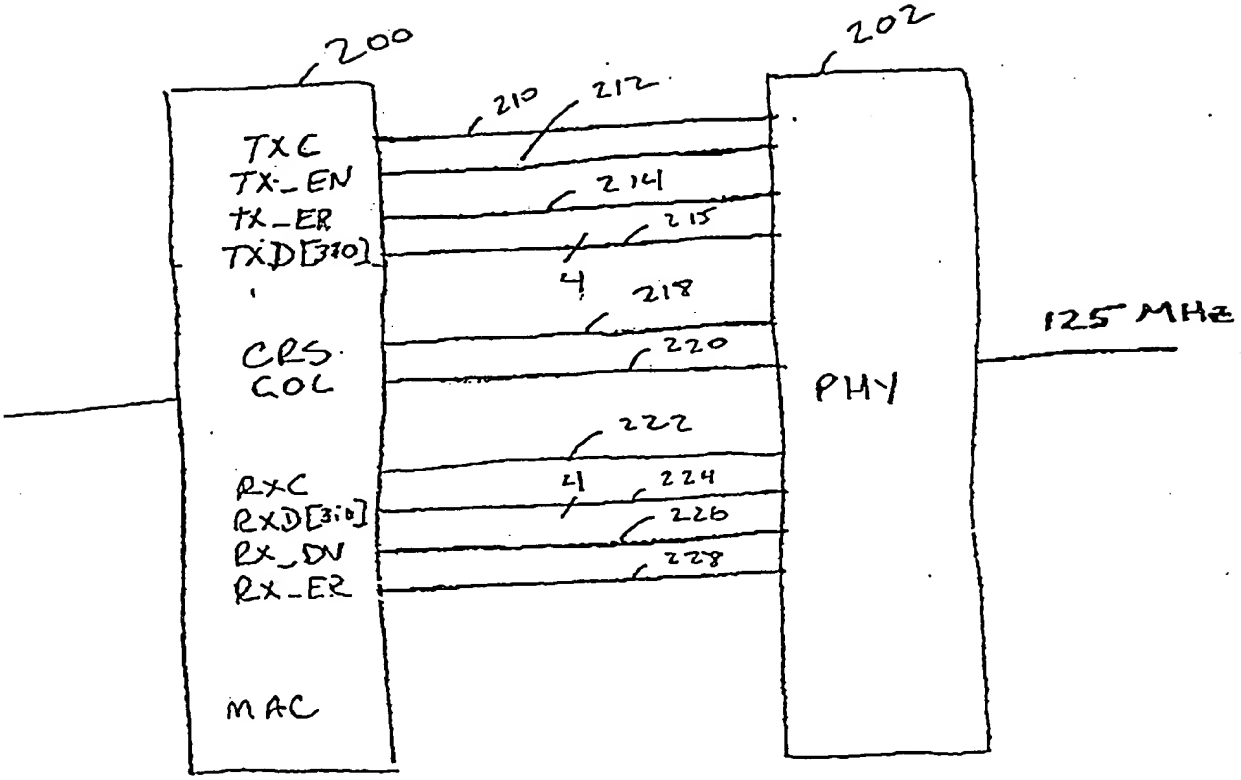
200
202
210
212
214
215
218
220
222
224
226
228
TXC
TX_EN
TX_ER
TXD[3:0]
4
CRS
COL
RXC
RXD[3:0]
4
RX_DV
RX_ER
MAC
PHY
125 MHz

Figure 2

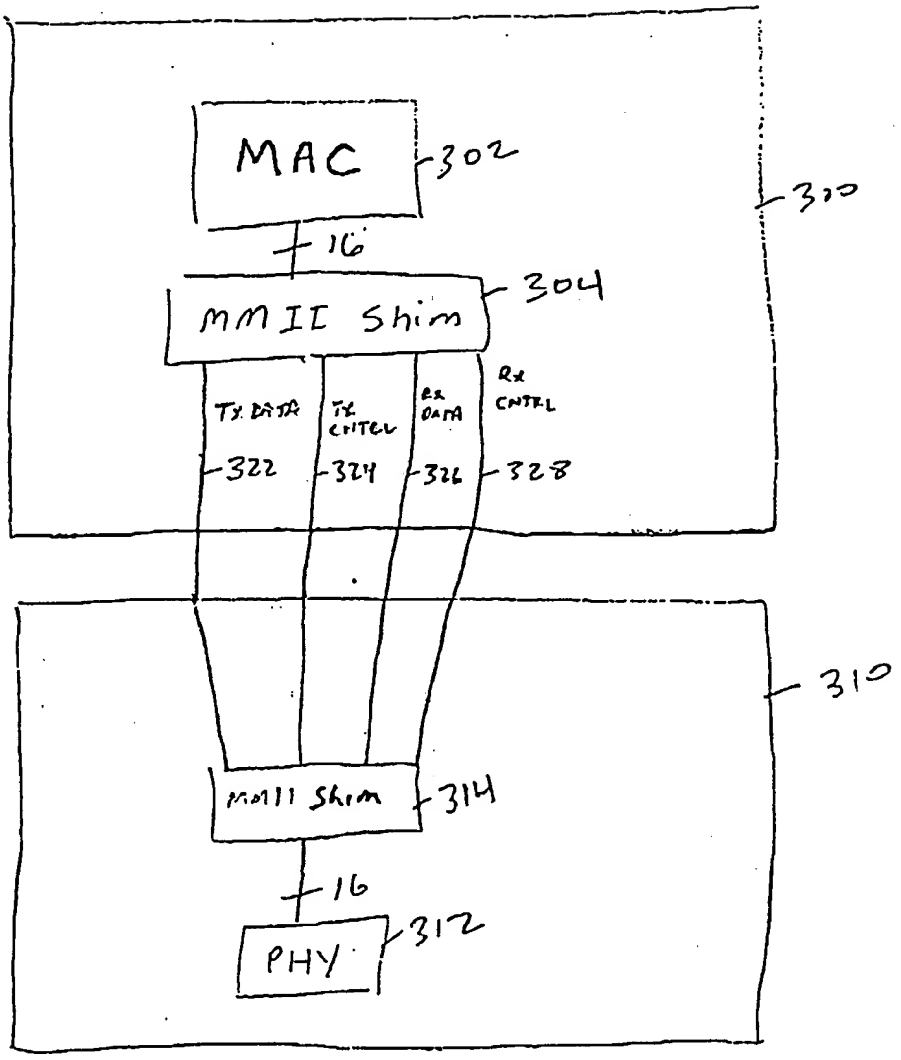

Figure 3

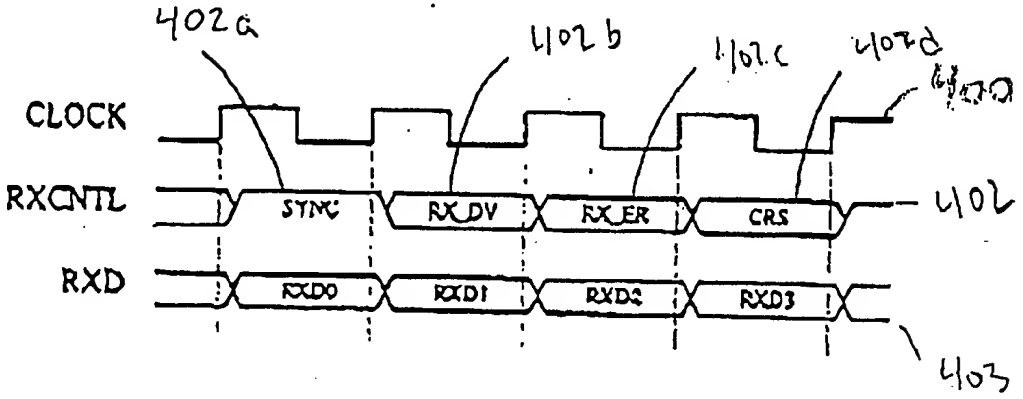

Figure 4

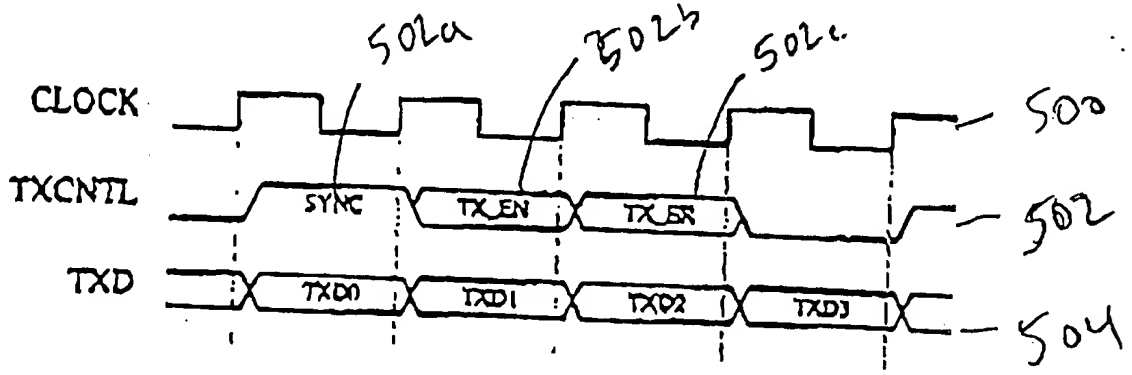
502a
502b
502c
CLOCK
TXCNTL
TXD
SYNC
TX_EN
TX_ER
TXD0
TXD1
TXD2
TXD3
500
502
504

FIGURE 5

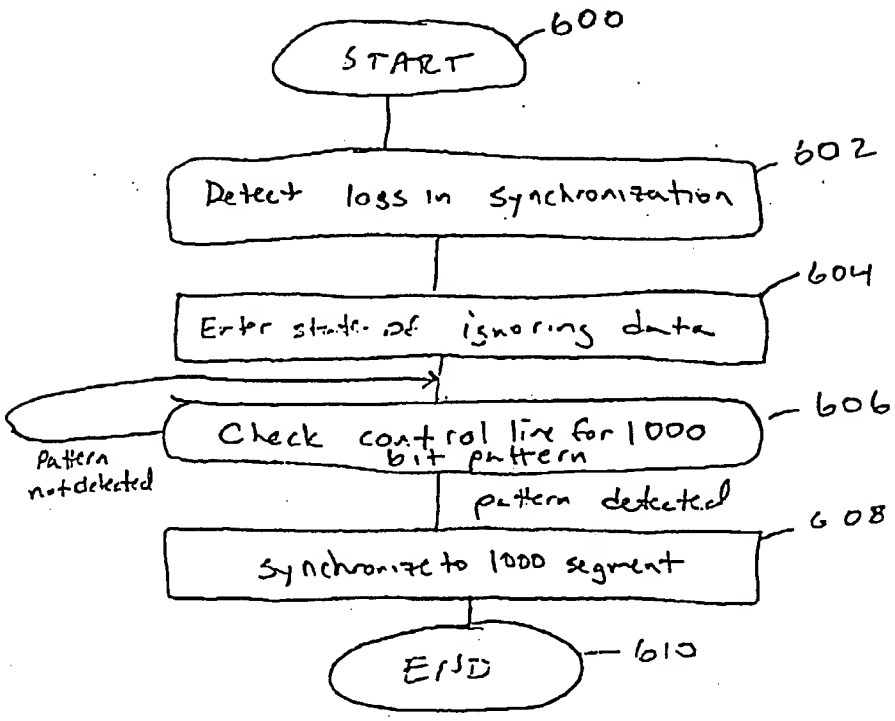
600
START
602
Detect loss in Synchronization
604
Enter state of ignoring data
606
Check control line for 1000 bit pattern
Pattern not detected
pattern detected
608
Synchronize to 1000 segment
END
610

Figure 6

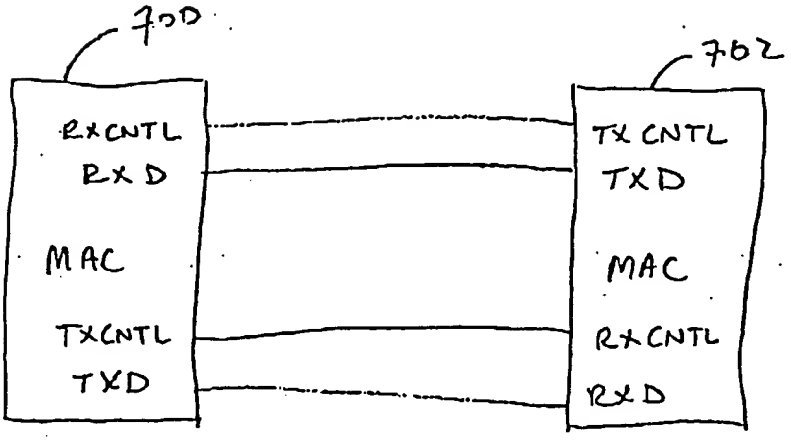

Figure 7